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EXAMINER

DHARIA, PRABODH M

ART UNIT PAPER NUMBER

2673

DATE MAILED: 04/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/099,994

Applicant(s)

KONNO ET AL.

Examiner

Prabodh M Dharja

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 June 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9,23,43,44 and 53-61 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9,23,43,44 and 53-61 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

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Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:

- (1) if a machine or apparatus, its organization and operation;
- (2) if an article, its method of making;
- (3) if a chemical compound, its identity and use;
- (4) if a mixture, its ingredients;
- (5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

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The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. It is a mere translation of a foreign language. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 60,61 are rejected under 35 U.S.C. 102(e) as being anticipated by Inoue et al. (US 2002/0154104 A1).

Regarding Claim 60, Inoue et al. teaches a liquid crystal display apparatus (page 4, paragraph 61, Lines 3,4) preset writing is executed on a full surface of a screen in synchronization with a frame signal (page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12), the image is made visible by intermittently lighting an illuminator, both polarities, positive and negative, are displayed in one frame period (page 12, paragraph 161, Lines 1-12, , a period obtained by subtracting a preset displaying period of each line from the one frame period (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16) is substantially equally distributed between positive polarity displaying and negative polarity displaying of one line, and then displaying is carried out (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16, page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12).

Regarding Claim 61, Inoue et al. teaches a liquid crystal display apparatus (page 4, paragraph 61, Lines 3,4) preset writing is executed on a full surface of a screen in synchronization with a frame signal (page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12), a first writing period, a first holding period, a second writing period, and a second holding period, to be driven in this sequence, reverse writing voltage polarities of the first and second writing periods, and set the second writing period to be about 1/2 of the first writing period (page 10, paragraph 133-136).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-9,23,42-44,53-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US 2002/0154104 A1) in view of Shiotani et al. (JP 2000-293142) and Takatori et al. (JP 11-237606).

Regarding Claim 1, Inoue et al. teaches a liquid crystal display apparatus (page 4, paragraph 61, Lines 3,4) comprising: a liquid crystal layer (page 4, paragraph 61, Lines 3,4,5) held between a pair of substrates (page 4, paragraph 61, Lines 5,6), at least one thereof being transparent (page 4, paragraph 61, Line 10); a plurality of line wirings (page 4, paragraph 62, Lines 2,3) and a plurality of column wirings (page 4, paragraph 62, Lines 3,4) disposed on one of the substrates; and first active elements in intersections of the plurality of line wirings and the plurality of column wirings (page 4, paragraph 61, Lines 12-14, page 4, paragraph 62, Lines 1-6), wherein an image is displayed by writing image data in pixels disposed in a matrix form through the first active elements (page 1, paragraph 3), preset writing is executed on a full surface of a screen in synchronization with a frame signal (page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12), the image is made visible by intermittently lighting an illuminator, both polarities, positive and negative, are displayed in one frame period (page 12, paragraph 161, Lines 1-12, , a period obtained by subtracting a preset displaying period of each line from the one frame period (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16) is substantially equally distributed between positive polarity displaying and negative polarity

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displaying of one line, and then displaying is carried out (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16, page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12).

However, Inoue et al. fails to teach specifically or recite the image is made visible by intermittently lighting an illuminator.

However, Shiotani teaches preset writing is executed on a full surface of a screen in synchronization with a frame signal (page 7, paragraph 20, Lines 5-17), the image is made visible by intermittently lighting an illuminator (page 7, paragraph 21, Lines 1-3, 8-13), both polarities, positive and negative, are displayed in one frame period (page 6, paragraph 16), a period obtained by subtracting a preset displaying period of each line from the one frame period is substantially equally distributed between positive polarity displaying and negative polarity displaying of one line, and then displaying is carried out (page 6, paragraph 17, Lines 2-11, page 7, paragraph 17, Lines 1-4).

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Shiotani in to the Inoue et al. teaching, to be able to raise display capacity at the time of displaying a dynamic image on a liquid crystal screen and display a quality image on a liquid crystal display screen.

Inoue et al. teaches a liquid crystal display apparatus (page 4, paragraph 61, Lines 3,4) comprising: a liquid crystal layer (page 4, paragraph 61, Lines 3,4,5) held between a pair of substrates (page 4, paragraph 61, Lines 5,6), at least one thereof being transparent (page 4, paragraph 61, Line 10); a plurality of line wirings (page 4, paragraph 62, Lines 2,3) and a plurality of column wirings (page 4, paragraph 62, Lines 3,4) disposed on one of the substrates; and first active elements in intersections of the plurality of line wirings and the plurality of

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column wirings (page 4, paragraph 61, Lines 12-14, page 4, paragraph 62, Lines 1-6), wherein an image is displayed by writing image data in pixels disposed in a matrix form through the first active elements (page 1, paragraph 3), preset writing is executed on a full surface of a screen in synchronization with a frame signal (page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12), the image is made visible by intermittently lighting an illuminator, both polarities, positive and negative, are displayed in one frame period (page 12, paragraph 161, Lines 1-12, , a period obtained by subtracting a preset displaying period of each line from the one frame period (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16) is substantially equally distributed between positive polarity displaying and negative polarity displaying of one line, and then displaying is carried out (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16, page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12).

However, Inoue et al. fails to teach one frame period is divided into a first writing period, a first holding period, a second writing period, a second holding period, and a reset writing period, the liquid crystal display apparatus is driven in this sequence, voltage polarities of the first and second writing periods are reversed, and the second writing period is set to be about 1/2 of the first writing period.

However, Takatori et al. teaches one frame period is divided into a first writing period, a first holding period, a second writing period, a second holding period, and a reset writing period, the liquid crystal display apparatus is driven in this sequence, voltage polarities of the first and second writing periods are reversed, and the second writing period is set to be about 1/2 of the first writing period (page 6, paragraph 18-22, page 7, paragraph 24, page 11, paragraph 43, paragraph 44).

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Takatori et al. in to the Inoue et al. teaching, to be able to raise display capacity at the time of displaying a dynamic image on a liquid crystal screen and display a quality image on a liquid crystal display screen by obtaining uniform in-surface luminance distribution and excellent contrast with less components per system.

Regarding Claim 2, Inoue et al. teaches a liquid crystal display apparatus (page 4, paragraph 61, Lines 3,4) comprising: a liquid crystal layer (page 4, paragraph 61, Lines 3,4,5) held between a pair of substrates (page 4, paragraph 61, Lines 5,6), at least one thereof being transparent (page 4, paragraph 61, Line 10); a plurality of line wirings (page 4, paragraph 62, Lines 2,3) and a plurality of column wirings (page 4, paragraph 62, Lines 3,4) disposed on one of the substrates; and first active elements in intersections of the plurality of line wirings and the plurality of column wirings (page 4, paragraph 61, Lines 12-14, page 4, paragraph 62, Lines 1-6), wherein an image is displayed by writing image data in pixels disposed in a matrix form through the first active elements (page 1, paragraph 3), preset writing is executed on a full surface of a screen in synchronization with a frame signal (page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12), the image is made visible by intermittently lighting an illuminator, both polarities, positive and negative, are displayed in one frame period (page 12, paragraph 161, Lines 1-12, , a period obtained by subtracting a preset displaying period of each line from the one frame period (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16) is substantially equally distributed between positive polarity displaying and negative polarity

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displaying of one line, and then displaying is carried out (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16, page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12).

However, Inoue et al. fails to teach specifically or recite the image is made visible by intermittently lighting an illuminator.

However, Shiotani teaches preset writing is executed on a full surface of a screen in synchronization with a frame signal (page 7, paragraph 20, Lines 5-17), the image is made visible by intermittently lighting an illuminator (page 7, paragraph 21, Lines 1-3, 8-13), both polarities, positive and negative, are displayed in one frame period (page 6, paragraph 16), a period obtained by subtracting a preset displaying period of each line from the one frame period is substantially equally distributed between positive polarity displaying and negative polarity displaying of one line, and then displaying is carried out (page 6, paragraph 17, Lines 2-11, page 7, paragraph 17, Lines 1-4).

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Shiotani in to the Inoue et al. teaching, to be able to raise display capacity at the time of displaying a dynamic image on a liquid crystal screen and display a quality image on a liquid crystal display screen.

Inoue et al. teaches a liquid crystal display apparatus (page 4, paragraph 61, Lines 3,4) comprising: a liquid crystal layer (page 4, paragraph 61, Lines 3,4,5) held between a pair of substrates (page 4, paragraph 61, Lines 5,6), at least one thereof being transparent (page 4, paragraph 61, Line 10); a plurality of line wirings (page 4, paragraph 62, Lines 2,3) and a plurality of column wirings (page 4, paragraph 62, Lines 3,4) disposed on one of the substrates; and first active elements in intersections of the plurality of line wirings and the plurality of

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column wirings (page 4, paragraph 61, Lines 12-14, page 4, paragraph 62, Lines 1-6), wherein an image is displayed by writing image data in pixels disposed in a matrix form through the first active elements (page 1, paragraph 3), preset writing is executed on a full surface of a screen in synchronization with a frame signal (page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12), the image is made visible by intermittently lighting an illuminator, both polarities, positive and negative, are displayed in one frame period (page 12, paragraph 161, Lines 1-12, , a period obtained by subtracting a preset displaying period of each line from the one frame period (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16) is substantially equally distributed between positive polarity displaying and negative polarity displaying of one line, and then displaying is carried out (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16, page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12).

However, Inoue et al. fails to teach one frame period is divided into a first writing period, a first holding period, a second writing period, a second holding period, and a reset writing period, the liquid crystal display apparatus is driven in this sequence, voltage polarities of the first and second writing periods are reversed, and the second writing period is set to be about 1/2 of the first writing period.

However, Takatori et al. teaches one frame period is divided into a first writing period, a first holding period, a second writing period, a second holding period, and a reset writing period, the liquid crystal display apparatus is driven in this sequence, voltage polarities of the first and second writing periods are reversed, and the second writing period is set to be about 1/2 of the first writing period (page 6, paragraph 18-22, page 7, paragraph 24, page 11, paragraph 43, paragraph 44).

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Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Takatori et al. in to the Inoue et al. teaching, to be able to raise display capacity at the time of displaying a dynamic image on a liquid crystal screen and display a quality image on a liquid crystal display screen by obtaining uniform in-surface luminance distribution and excellent contrast with less components per system.

Regarding Claim 3, Takatori et al. teaches the second writing period is started after a passage of about $1/2$ of a period obtained by subtracting a presetting period from one frame period (page 8, paragraph 32, Lines 1-9).

Regarding Claim 4, Takatori et al. teaches the first holding period is set to be substantially zero (page 8, paragraph 32, Lines 1-11).

Regarding Claim 5, Takatori et al. teaches each writing period, writing polarities are similar to each other on a full surface of the screen (page 11, paragraph 43, paragraph 44).

Regarding Claim 6, Inoue et al. teaches a potential of a common electrode as a reference for a potential a pixel wiring is varied between the first and second writing periods (page 1, paragraph 9, page 5, paragraph 63, Lines 16-19).

Regarding Claim 7, Takatori et al. teaches a second holding period and a lighting period of the illuminator are substantially equal to each other (page 12, paragraph 45, Lines 3-10).

Regarding Claim 8, Shiotani teaches a lighting period of the illuminator, all the column wirings are fixed to predetermined potentials (page 6, paragraph 16).

Regarding Claim 9, Takatori et al. teaches the predetermined potentials is one selected from a black-displaying potential and a displaying potential of a slow optical response speed (page 7, paragraph 24-26).

Regarding Claim 23, Inoue et al. teaches a liquid crystal display apparatus (page 4, paragraph 61, Lines 3,4) comprising: a liquid crystal layer (page 4, paragraph 61, Lines 3,4,5) held between a pair of substrates (page 4, paragraph 61, Lines 5,6), at least one thereof being transparent (page 4, paragraph 61, Line 10); a plurality of line wirings (page 4, paragraph 62, Lines 2,3) and a plurality of column wirings (page 4, paragraph 62, Lines 3,4) disposed on one of the substrates; and first active elements in intersections of the plurality of line wirings and the plurality of column wirings (page 4, paragraph 61, Lines 12-14, page 4, paragraph 62, Lines 1-6), wherein an image is displayed by writing image data in pixels disposed in a matrix form through the first active elements (page 1, paragraph 3), preset writing is executed on a full surface of a screen in synchronization with a frame signal (page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12), the image is made visible by intermittently lighting an illuminator, both polarities, positive and negative, are displayed in one frame period (page 12, paragraph 161, Lines 1-12, , a period obtained by subtracting a preset displaying period of each line from the one frame period (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16) is substantially equally distributed between positive polarity displaying and negative polarity

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displaying of one line, and then displaying is carried out (page 4, paragraph 56, Lines 1-4, page 7, paragraph 105, Lines 1-16, page 7, paragraph 20, Lines 5-17, page 12, paragraph 161, 1-12).

However, Inoue et al. fails to teach specifically or recite the image is made visible by intermittently lighting an illuminator.

However, Shiotani teaches preset writing is executed on a full surface of a screen in synchronization with a frame signal (page 7, paragraph 20, Lines 5-17), the image is made visible by intermittently lighting an illuminator (page 7, paragraph 21, Lines 1-3, 8-13), both polarities, positive and negative, are displayed in one frame period (page 6, paragraph 16), a period obtained by subtracting a preset displaying period of each line from the one frame period is substantially equally distributed between positive polarity displaying and negative polarity displaying of one line, and then displaying is carried out (page 6, paragraph 17, Lines 2-11, page 7, paragraph 17, Lines 1-4).

Thus it would have been obvious to one in the ordinary skill in the art at the time of invention was made to incorporate the teaching of Shiotani in to the Inoue et al. teaching, to be able to raise display capacity at the time of displaying a dynamic image on a liquid crystal screen and display a quality image on a liquid crystal display screen.

Regarding Claim 42, Inoue et al. teaches a black writing voltage of the second writing voltage is equal to/lower than a black writing voltage of the first writing period (page 3, paragraph 48, page 4, paragraph 52).

Regarding Claim 43, Inoue et al. teaches a writing polarity is set in order to set a potential difference between a high voltage V_{gh} and a voltage V_{dbk2} for black displaying during gate writing in the second writing period larger than a potential difference between a high voltage V_{gh} and a voltage V_{dbk1} for black displaying during gate writing in the first writing period (page 3, paragraph 48, page 4, paragraph 52, 53).

Regarding Claim 44, Takatori et al. teaches the reset writing is black writing (page 6, paragraph 13).

Regarding Claim 53, Inoue et al. teaches a display mode of the liquid crystal is an in-plane switching mode or a normally black mode, on which displaying is black when no voltage is applied to the liquid crystal (page 3, paragraph 48, page 4, paragraph 52, 53).

Regarding Claim 54, Shiotani teaches the first active element for writing in the pixel is a high-mobility active element (page 4, paragraph 05).

Regarding Claim 55, Inoue et al. teaches the high-mobility active element is a polycrystal thin film transistor or a single crystal silicon transistor (page 4, paragraph 61).

Regarding Claim 56, Inoue et al. teaches the common wirings are disposed in a meshed form (page 4, paragraph 61, 62).

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Regarding Claim 57, Inoue et al. teaches the common wirings are disposed in parallel with the column wirings (page 12, paragraph 166,167).

Regarding Claim 58, Shiotani teaches the illuminator uses a high-speed response light source (page 7, paragraph 20).

Regarding Claim 59, Shiotani teaches the high-speed response light source is one selected from, or a combination of a light source using a field emission electron source (FED: field emission display), a light source of a plasma using emission type, a high-speed response fluorescent tube (page 7, paragraph 20,21, page 6, paragraph 16).

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is informed that all of the other additional cited references either anticipate or render the claims obvious. In order to not to be repetitive and exhaustive, the examiner did draft additional rejection based on those references.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kawabe et al. (US 2003/0169247 A1) Display device having improved drive circuit and method of driving same.

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11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 703-605-1231.

The examiner can normally be reached on M-F 8AM to 5PM.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-3054938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

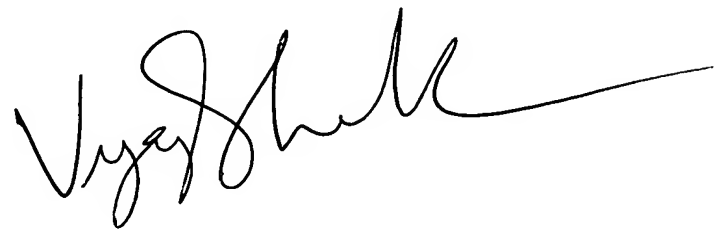
Commissioner of Patents and Trademarks

Washington, D.C. 20231

PD

AU2673

July 15, 2044

A handwritten signature in black ink, appearing to read 'Vijay Shankar', with a long horizontal flourish extending to the right.

**VIJAY SHANKAR
PRIMARY EXAMINER**